CLAIMS

What is claimed is:

1. A semiconductor device in which one or more semiconductor chips have been mounted onto one or more substrates incorporating patterned wiring and the entirety or entireties has or have been sealed with one or more resins, wherein:

one or more electrically conductive patterns for shielding is or are formed at one or more end faces at the top of at least one of the substrate or substrates.

2. A semiconductor device according to claim 1 wherein:

at least one of the electrically conductive pattern or patterns is at least one copper foil pattern.

3. A semiconductor device according to claim 2 wherein:

at least one plating having good shielding characteristics is applied over at least one of the copper foil pattern or patterns.

4. A semiconductor device according to claim 3 wherein:

at least one of the plating or platings is gold plating.

5. A semiconductor device according to any of claims 2 through 4 wherein:

one or more shield cases is or are attached over at least one of the electrically conductive pattern or patterns by way of one or more intervening electrically conductive adhesives.

6. A semiconductor device according to claim 5 wherein:

at least one of the shield case or cases is gold-plated.

7. A semiconductor device according to claim 4 or 6 wherein:

one or more shield cases is or are attached over at least one of the electrically conductive pattern or patterns by way of one or more intervening silver pastes.

8. A semiconductor device in which one or more semiconductor chips have been mounted onto one or more substrates incorporating patterned wiring and the entirety or entireties has or have been sealed with one or more resins, wherein:

one or more electrically conductive patterns is or are formed at one or more end faces at the bottom of at least one of the substrate or substrates; and

at least as many terminal or terminals of such number, size, and shape as is or are

sufficient for connection to the patterned wiring is or are formed by using one or more dies to blank out and shape at least one region at or in the vicinity of at least one of the electrically conductive pattern or patterns.

9. A semiconductor device according to claim 8 wherein:

at least one of the terminal or terminals is formed so as to at least partially protrude to the exterior and so as to have at least one more or less rectangular cross-section.

10. A semiconductor device according to claim 8 or 9 wherein:

at least one gold plating is applied to at least one end face of at least one of the terminal or terminals.

11. A semiconductor device manufacturing method comprising:

forming a plurality of patterned wiring fields horizontally and vertically on one or more substrates, at least one of the fields containing patterned wiring for connection to one or more semiconductor chips;

mounting at least one of the semiconductor chips or chips to at least one of the patterned wiring fields;

sealing the entirety of at least one of the mounted semiconductor chips or chips with one or more resins;

thereafter forming at least one vertically long set of at least two through-holes in more or less parallel fashion with respect to at least one region at or in the vicinity of at least one end face at at least one side corresponding to at least one top and with respect to at least one region at or in the vicinity of at least one end face at at least one side corresponding to at least one bottom of each of at least one of the semiconductor chip or chips;

applying plating to at least a portion of the interior of at least one of the through-hole or through-holes;

forming one or more electrically conductive patterns;

thereafter using one or more dies to blank out and shape at least one region at or in the vicinity of at least a portion of the through-holes and containing at least one region at or in the vicinity of at least one of the electrically conductive pattern or patterns formed in at least one region at or in the vicinity of at least one of the end face or faces at at least one of the side or sides corresponding to at least one of the bottom or bottoms of at least

one of the semiconductor chip or chips so as to form one or more electrically conductive patterns for shielding at or in the vicinity of at least one of the end face or faces at at least one of the side or sides corresponding to at least one of the top or tops of at least one of the semiconductor chip or chips, and so as to form at least as many terminal or terminals of such number, size, and shape as is or are required for at least one region at or in the vicinity of at least one of the end face or faces at at least one of the side or sides corresponding to at least one of the bottom or bottoms of at least one of the semiconductor chip or chips; and

thereafter cutting in one or more directions perpendicular to at least one of the vertically long set or sets of through-holes so as to divide substantially the entirety into a plurality of individual semiconductor devices.

12. A semiconductor device manufacturing method according to claim 11 further comprising:

attaching one or more shield cases over at least one of the electrically conductive pattern or patterns for shielding formed at or in the vicinity of at least one of the end face or faces at at least one of the side or sides corresponding to at least one of the top or tops of at least one of the semiconductor chip or chips by way of one or more intervening electrically conductive adhesives.